

Replacement Sheet

FIG. 1

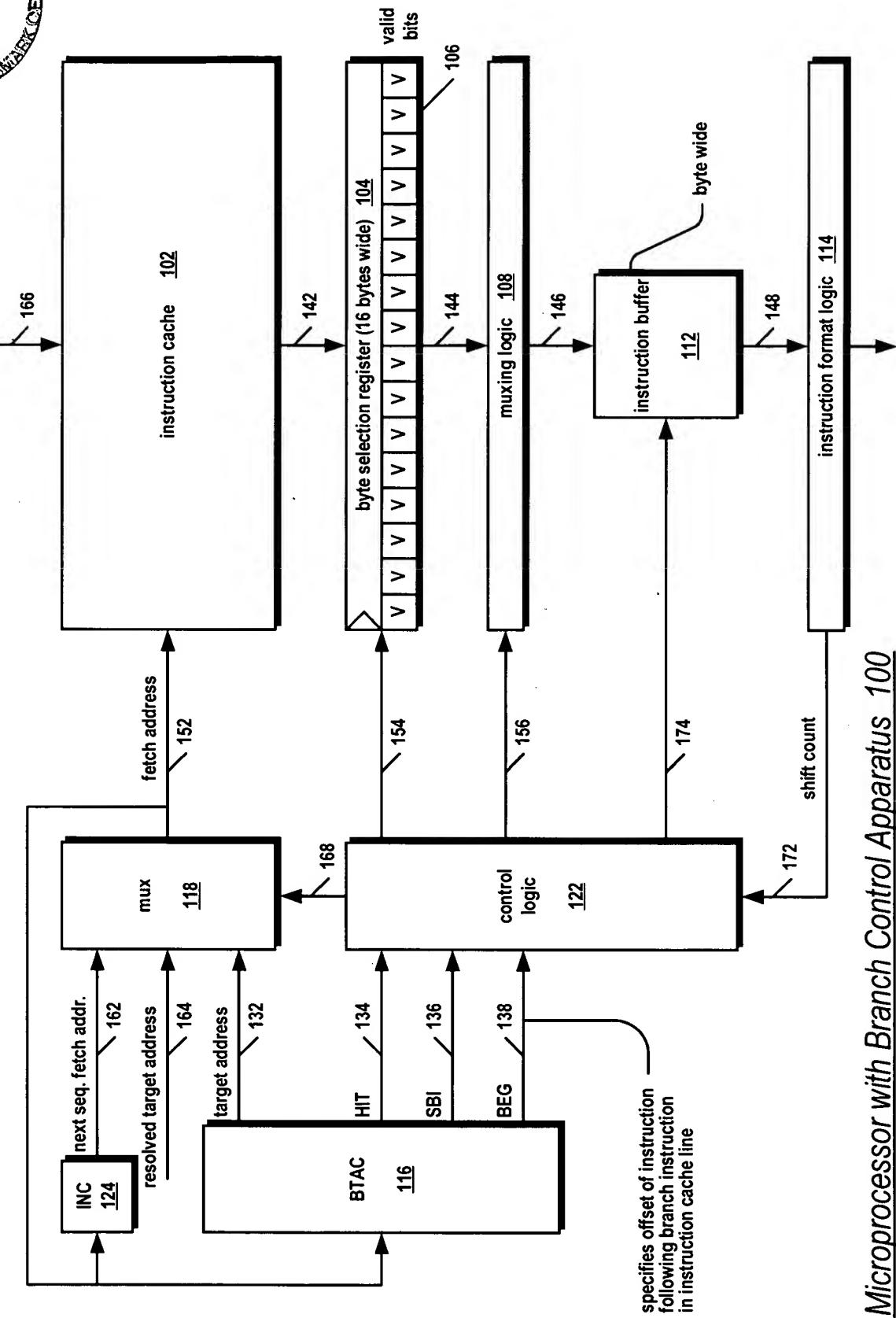
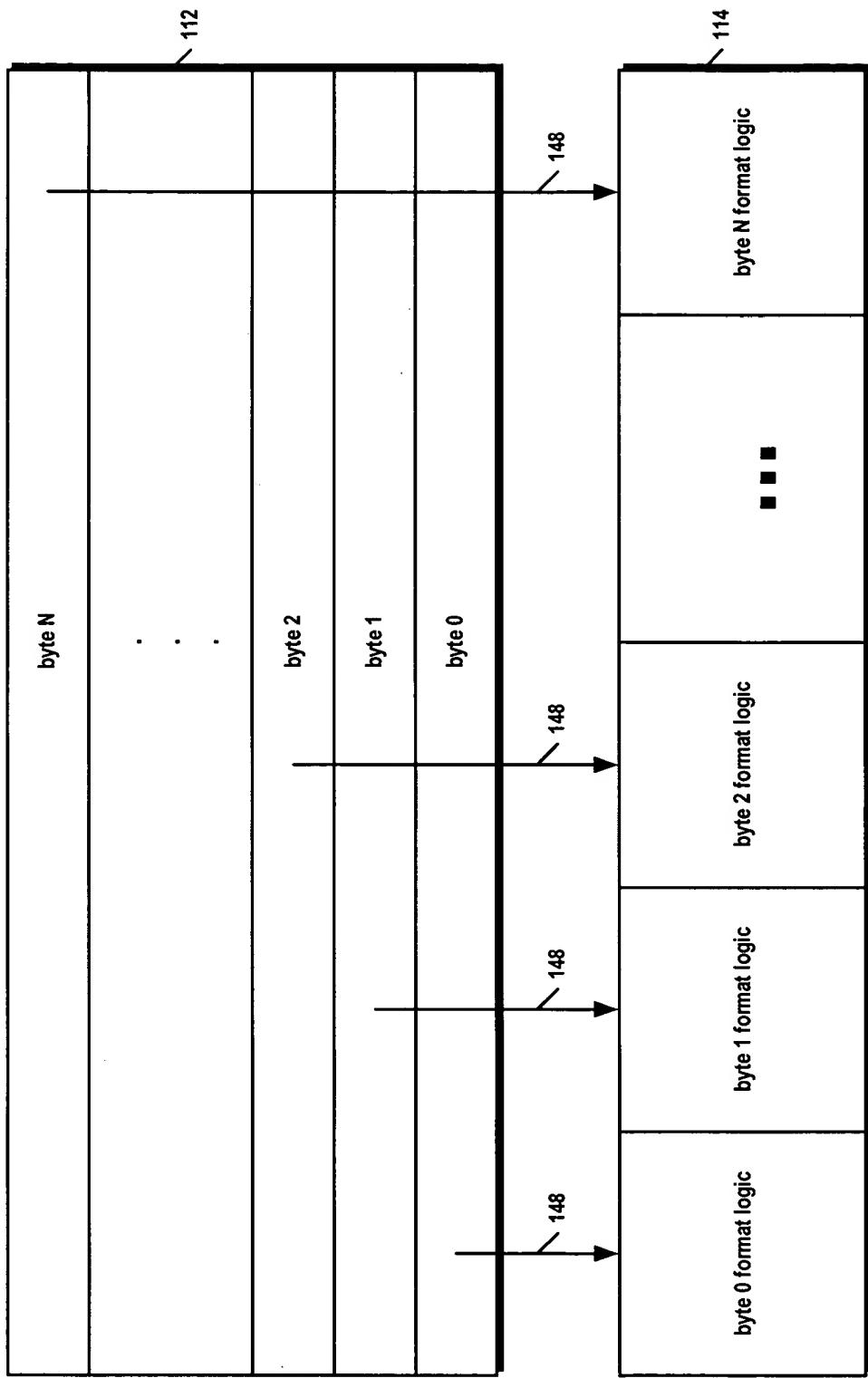


FIG. 2



Instruction Buffer to Instruction Format Logic Coupling 100

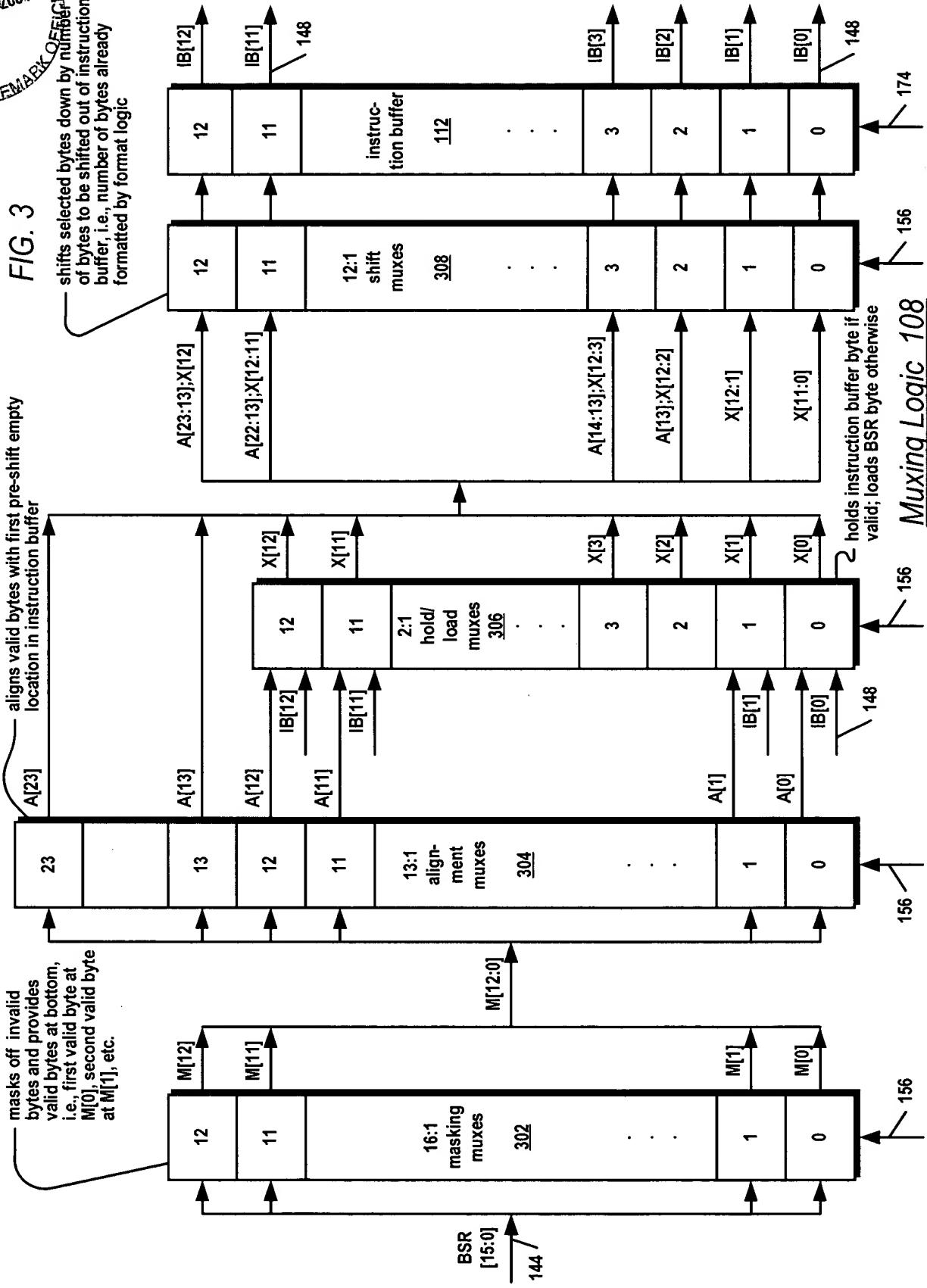


Replacement Sheet

FIG. 3

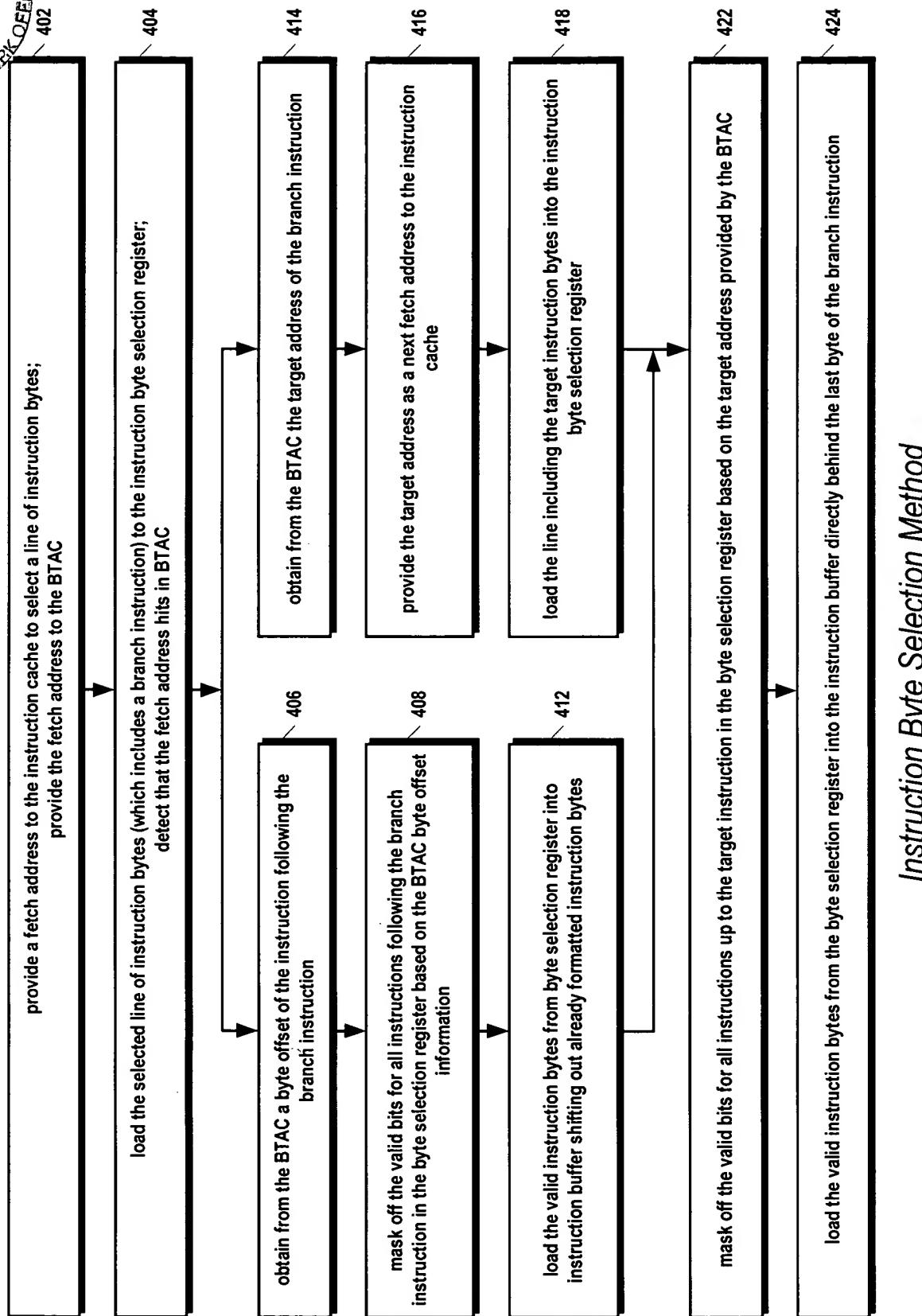
- aligns valid bytes with first pre-shift empty location in instruction buffer

masks off invalid bytes and provides valid bytes at bottom, i.e., first valid byte at $M[0]$, second valid byte at $M[1]$, etc.



Replacement Sheet

FIG. 4





Replacement Sheet

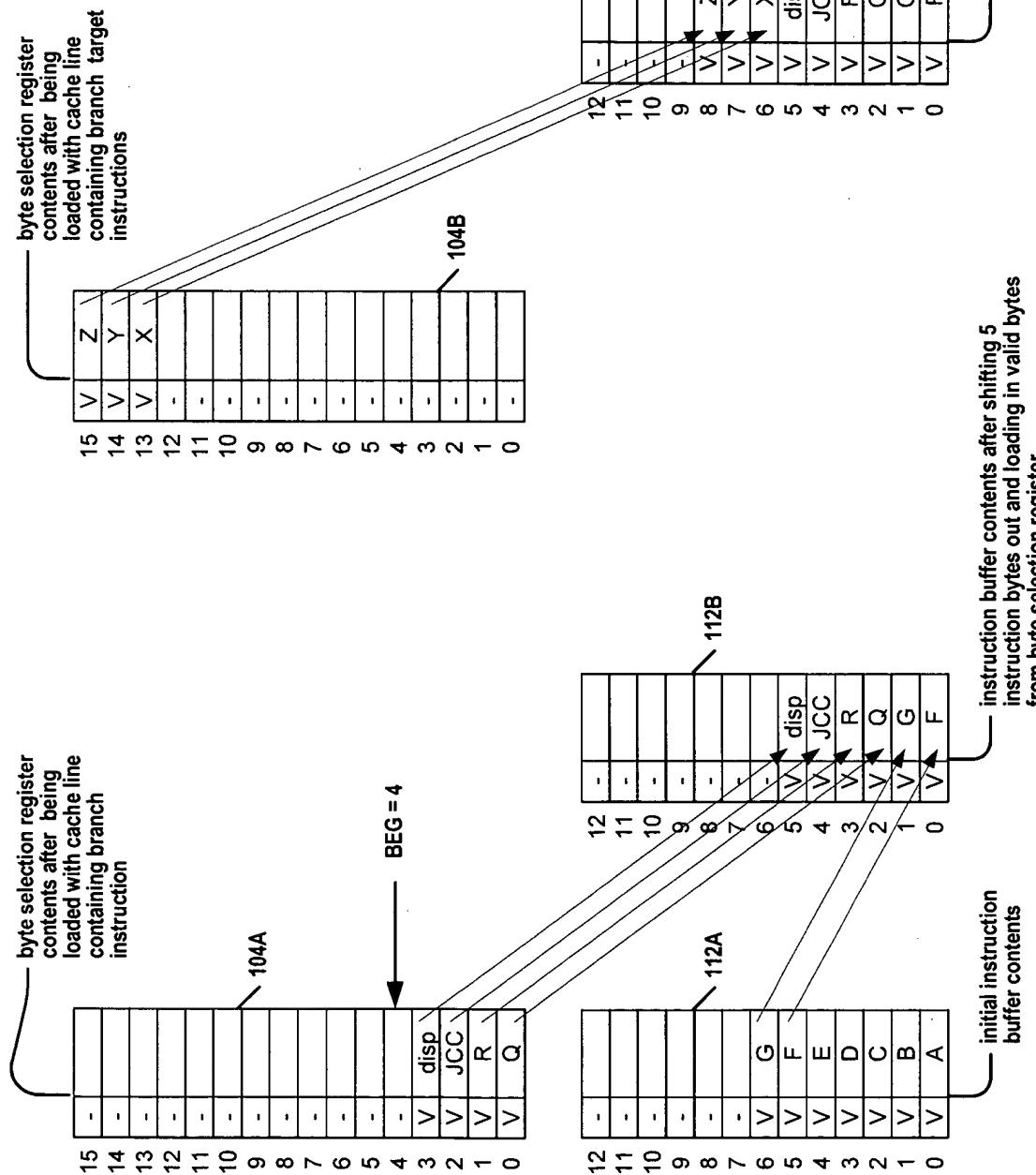


FIG. 5

Branch Control Apparatus Operation Example